Options for Radiation Tolerant High-Performance Memory

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***Abstract*— Memory technologies were reviewed for radiation effects performance in order to determine the most cost-efficient target for a possible memory investment targeted at creating a memory component of general applicability for space use. TID and SEL trends that had indicated improvement in intrinsic performance based on scaling cannot be trusted. SEE hardening of memory arrays is prohibitive in terms of cell-level power and area requirements. Radiation-hardened cells and custom controllers are recommended for future memory developments.**

I. Introduction

Space missions require memory for many different applications, including computer main memory, buffers, program and data storage, boot ROMs (read only memory), and other applications. In the specific cases of high density volatile memory (currently handled with dynamic random-access memory [DRAM] devices), and high density non-volatile memory (currently handled with Flash memory), it was determined that total ionizing dose (TID) and single-event effects (SEE) performance were insufficient for high-reliability deep space systems. A comprehensive review of available memory technologies, coupled with a review of their radiation performance, will help identify the memory technologies with the most potential to benefit from a modest effort to develop a next-generation radiation hardened memory technology.

Radiation performance trends for technologies and devices provide key information about current and future expectations. Potential high-performance radiation hardened memory devices include radiation hardened by design devices, commercial devices, and hybrids. In this paper, we review radiation hardened by design (RHBD) libraries as well as fabrication options, expected performance, and limitations. In addition, we provide a technology review of a range of advanced memory technologies and their expected radiation performance into the future. These analyses provide a basis from which it will be possible to identify if high-performance deep space memory requirements can be met now, in the future, or in the future with the addition of targeted development to remedy specific shortcomings of predicted performance.

This paper is a formal review of RHBD and commercial technologies of potential use for development of a space memory. The goals of this paper, are to:

- Use appropriate radiation environments for evaluation of radiation effects in memory devices and technologies.
- Review available RHBD options and assess radiation performance.
- Identify impact of RHBD limitations, especially at low feature size.
- For each memory technology, identify cell-level radiation performance strengths and weaknesses.
- Identify specific trends in memory controller strengths and weaknesses (i.e. Flash memory charge pumps).
- Identify any other strengths or weaknesses of note for memory technologies.
- Ensure the memory technologies are single-event latchup (SEL) free.
- Identify memory technologies that can provide DRAM-like performance and/or Flash-memory like performance, while meeting single- and multiple-bit upset (SBU and MBU) and SEFI rate requirements (with SEFI being the more problematic).

The approach taken for this work was the following. We took two generic space environments – one that was heavy-ion dominated, and one that was proton dominated. We identified the available RHBD suppliers and evaluated the performance of their RHBD libraries. We then identified memory technologies and their radiation performance and trends. With the last several generations of performance as a starting point, we projected technology trends into the future for memory devices.

This summary is organized as follows. Background is presented in Section II. Environments considered for this work are presented in Section III. A review of RHBD programs is presented in Section IV. Reviews of individual memory trends is presented in Section V. An exploration of packaging impact on radiation response is presented in Section VI. And finally, the findings are presented in Section VII.

II. Background

The following general assumptions are made in order to focus this work:

1) The general timeframe targeting a future improved product is about 2-4 years. Significant findings that seem to require more than 4 years are noted but not pursued here. Our focus in then on memory technology predictions in the next few years only.

2) Device densities of 256 Mb or larger are required for deep space missions. Smaller density devices (and developing cell technologies) are not fully explored.

3) Feature size must be 65 nm or smaller for the required density.

4) The types of memories of interest are limited to the following: static random-access ram (SRAM), dynamic RAM (DRAM), NAND Flash, NOR Flash, magnetic RAM

(MRAM), spin-torque transfer (STT), ferro-electric RAM (FeRAM), phase change RAM (PCRAM), and resistive RAM (RRAM).

5) The types of radiation effects of the greatest concern are the following: TID, SBU, MBU, SEFI, SEL, Stuck Bits, and Other types of permanent failures

6) We identified two use categories of the greatest concern – high speed memory to act as computer main memory, and high density non-volatile memory to act as file system storage.

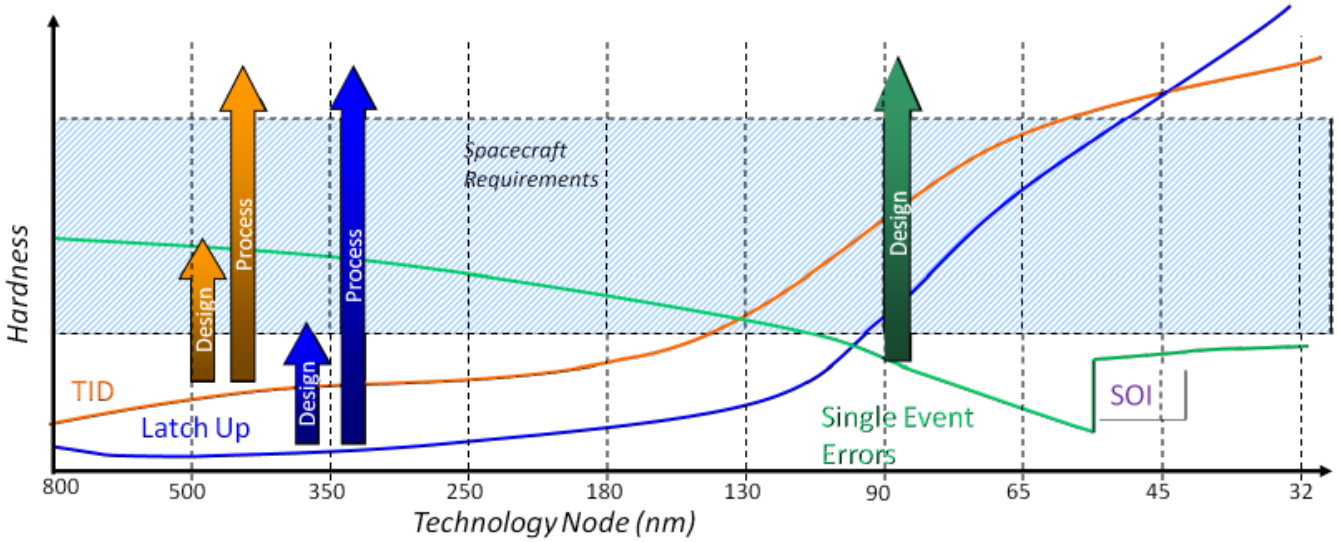

Figure 1: Commercial trends and methods to improve hardness, per Amort [1]. There are some notable examples that deviate from the predicted SEE and TID trend lines. Also, this is changing in the sub-32 nm range as mixed-signal and process changes are making this only a rough guideline.

III. Environments

For this paper, we focused on technology performance under a subset of key mission environments. These are the following: low-earth orbit (LEO) at 51.6° inclination is the International Space Station orbit (ISS) [2]; geo-stationary orbit (GEO); and interplanetary space. GEO orbit includes a portion of the upper Van-Allen belts and thus has a slightly higher TID component than interplanetary space [3]. The main difference between the latter environments, as it pertains to mission radiation exposure is that GEO has somewhat higher TID levels and generally has SEE rates between ISS and interplanetary space. For reference, TID rates are around 500 rad(Si)/year in LEO and 1-10 krad(Si)/year in GEO (depending on orbit, solar cycle, and other factors). The TID targets we were primarily interested in were 100 krad(Si) minimum, and a desired capability of 300 krad(Si).

IV. RHBD Options

It is possible to make standard components perform better in radiation environments by altering low-level library element designs (e.g. by adding in feedback loops), altering higher level functionality (like triple module redundancy [TMR]), or by changing the thickness of material stacks or using alternate materials. The collection of all these methods is referred to as radiation hardening by design. That is, by just informing the fabrication facility to construct a device differently, radiation performance can be improved (as opposed to modifying the actual process the facility uses, which has been termed "radiation hardening by process"). There are a handful of suppliers that can create new integrated circuits (ICs) or modify their commercial designs, using RHBD methods.

For this effort, it is important to be informed of RHBD-supplied memories and how they fit requirements. RHBD capabilities and available densities (related to feature size) are also important. With this information, it is possible to establish the state of the art for memory constructed using RHBD methods, where those efforts are likely to lead in the future, and whether a custom development using RHBD is feasible.

In this review, we explore the rad hard by design programs listed below. Each of the programs has been reviewed and the findings are discussed.

1) Boeing 90 nm – as a baseline
2) Cobham 65 nm
3) BAE 45 nm
4) Boeing 32 nm

A. *Boeing 90 nm*

The 90 nm Boeing RHBD program is an example of a well-document RHBD library that has been used to make ASICs. Some of the devices made in this technology node, such as the MAESTRO processor had to be implemented with lower-end RHBD in some areas due to the number of SRAM bits used and the lack of space to implement the bits on the device. 90 nm is considered too large for the desired device density but is used to establish trends. This library is considered mature, but it is also old and there is a successor in the newer 32 nm program from Boeing.

It is important to briefly discuss the observed memory SEE rate of 1×10^{-6}/bit-day in ISS and 5×10^{-6}/bit-day in solar minimum GCR. These are a few orders of magnitude poorer performance than bits from other RHBD programs reviewed

later. It is believed this happened because Boeing chose to implement better EDAC, along with partial hardening of cells, rather than full RHBD of cells. As a result, the rates for on-orbit errors in EDAC-protected memories is still very low (typically it can get down below 1×10^{-4}/system-year, with sufficient scrubbing). The results are summarized in Table 1.

The TID and SEL performance of the RHBD library developed on this fabrication line are both very good. However, this fabrication node may be at a sweet spot for both SEL and TID performance. Later devices use lower voltage, which helps with SEL. But the later devices are also using more complicated peripheral functions on-chip, which returns the risk for SEL. In the specific case of 90 nm, the node is too large to support 1 Gb devices (with die that can fit in standard DRAM outlines – it takes around 2 cm^2 for non-RHBD and around 50% more for RHBD cells of any type), so it cannot be used. Devices in later technology nodes also carry TID risk due to heterogeneous on-chip resources. Presumably the TID and SEL risks of heterogeneous structures is minimized when device design is intended for RHBD applications.

B. Cobham 65nm

Cobham/Aeroflex developed the STMicroelectronics 65 nm fabrication capability into an RHBD library and capable production supplier. In order to support this, they migrated library elements and improved radiation performance on some library elements. 65 nm is not an advanced enough node at this point for future developments and is considered only marginally acceptable. At the time of developing this information, there was an alternate, lower feature size, but details were not available. The Cobham information is based on the public data developed by ESA on the 65 nm STMicroelectronics fabrication capabilities. This fabrication plant has explicitly been a producer of DRAMs in the past.

The 65 nm fabrication capability here has been used by STMicroelectronics for production of parts for many years and is considered stable. The only real issue with this fabrication node is that the density will not be good enough. In point of fact, Cobham has apparently hit the lowest rates for SEFIs of all the manufacturers studied. But ultimately these are all within factors of 5-10. The findings are summarized below.

C. BAE 45nm

The 45 nm PDSOI program at BAE systems is currently at the cusp of producing the RAD55 series processors that will power the next generation of flight computers from BAE, such as the RAD5545 and RADSPEED. At 45 nm the fabrication facility is in line with the technology requirements memory effort (65 nm or below). At 45 nm, it is also true that RHBD library elements are less effective because ionization paths can swamp an entire circuit element rendering negative feedback structures less effective.

The BAE 45 nm key attribute is that they can improve the radiation hardness of the SRAM cells somewhat, making the overall bit error rate lower before error correction. Also, the non-RHBD version of their SRAM cells is about 10-50× better than the other RHBD providers. The program overview [1] provides significant information on baseline library elements. This library is not expected to migrate to a smaller feature size in the near future. So, the parameters in the table would be expected to hold for the next 3-5 years. The logic error/SEFI rate shows similar sensitivity between protons and heavy ions, suggesting that some SEFIs are caused by proton events (secondaries).

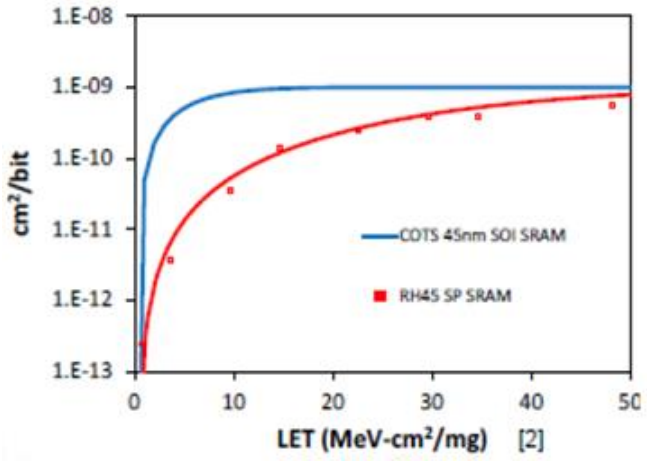

Figure 2: Commercial and BAE 45 nm SRAM SEE performance [5]. With these curves we can derive space rates of 1×10^{-9} upsets/bit-day for the RHBD cell, and 10×-50× higher for the COTS cell. But even at 1×10^{-9} upsets/bit-day EDAC is required for space programs.

D. Boeing 32nm

The 32 nm SOI RHBD program at Boeing is much newer than the 90 nm and promises to provide ASICs for the next several years or more. This node provides significantly increased density and is likely to be less power-hungry than the 90 nm node. It should be capable of providing the target density easily. This program has been used to create some devices over the last several years and is rapidly becoming mature.

The materials reviewed, and the findings indicate the performance of the 90 nm program was sufficient, and the 32 nm program has approximately the same performance numbers. Hence it appears to be of limited value to try to improve the library more. This is especially true since there are basically 10 circuit elements inside every circuit element from the 90 nm program. This suggests that the EDAC methods employed by Boeing are sufficient to reach the desired performance requirements. For this reason no clear difference is observed between 32 and 90 nm. It is likely that RHBD on SRAM and FF elements are less effective than in 90 nm, and clusters may actually be closer to 10-20 cells at a time.[1] It should also be noted that Boeing, from within their

[1] It should be noted that previous claims that numbers of bit errors per ion strike would increase dramatically as feature size goes down has not held to the extent portended.

32 nm development efforts implemented an eDRAM macro, which is reported in the technology template section.

E. RHBD Summary

Error correction is typically used to achieve 5 orders of magnitude improvement from bit-level with no correction. Thus, to achieve 1×10^{-10} errors per bit day level, the baseline raw error rate must not be above 1×10^{-5} raw rate. Boeing provides raw rates, BAE provides corrected rates. Cobham's error rates were unclear from specifications available to us during this study. Note that the Cobham findings presented are based on the 65 nm ST Micro process study done by ESA [4] and may be slightly different than rates actually achieved by Cobham's RHBD offerings.

BAE 45nm is indicated as having 20-50× improvement over commercial to RHBD. This is achieved by changing the cell-level sensitivity as indicated in Figure 2. Here it is shown that the RHBD efforts reduced the SEE sensitivity in the knee region but did not move the threshold nor the saturated cross section [5]. Because of the benefit being limited to the knee region, this does have a reasonable impact on rates, but the resulting rate of 1.2×10^{-9} cm^2 is still too high for a high reliability ISS mission, and EDAC is required to meet mission needs.

MFR & Tech/Name	Feature Size	TID (krad[Si]) Total	TID (krad[Si]) Functional	Memory SEE Rate (#/bit-day) ISS	Memory SEE Rate (#/bit-day) Inter.Plan. GCR	Logic/Alt SEE Rate (#/device-day) ISS	Logic/Alt SEE Rate (#/device-day) Inter.Plan. GCR
BAE 45nm Commercial	45 nm			1.40E-08	5.00E-08		
BAE 45nm RH	45 nm	1000	1000	1.20E-09	1.00E-09	1.00E-07	1.00E-07
Boeing 90nm	90 nm	>600	1000	1.00E-06	5.00E-06	2.00E-08	3.00E-07
Boeing 32nm	32 nm	>1000	3000	1.00E-06	1.00E-05	2.00E-08	3.00E-07
Aeroflex 65nm	65 nm	>300	>300	4.00E-07	4.00E-06	1.00E-09	2.00E-08

Table 1: Summary of rates developed from RHBD program information (Boeing 90nm [6][7], Cobham 65 nm [8], BAE 45 nm [9], Boeing 32 nm [10]).

The key findings of the RHBD study are the following:

1) Protons are becoming more problematic in newer, highly-scaled, RHBD circuits. This results in a larger portion of errors occurring in flare or MEO environments compared to traditional high LET environments (e.g. non-flare GEO or deep space). This is expected to worsen as feature size decreases. For the same level of traditional radiation hardness, scaled devices have more difficulty operating through a flare or meeting operational requirements in MEO.

2) Commercial SRAM cells are now very commonly used for high speed semi-bulk memory (in very high speed applications, they are often replaced with flip flops). This means that localized information storage, i.e. for use as scratch-pad memory, there is a high likelihood of being commercial SRAM, even in an RHBD part. These are very soft and can easily dominate a device's SEE response (1×10-7 upsets per bit day in LEO & GEO). See Figure 2.

3) Feature size is so small in state of the art technologies that older, spacing-based, hardening methods, like the dual-interlocked cell (DICE) are no longer sufficient in many cases. Thus it is expected that we will see increased SEE rates in low level RHBD circuits, and increased use of redundancy in an effort to mitigate these errors and reduce the overall system rate.

4) Another trend that appears to be developing is cross usage of fabrication facilities. In particular, it is expected that, at 32 nm and below, RHBD designers may share existing resources within the RHBD community, possibly using common third-party fabrication facilities.

5) Overall, there is a clear indication that memory arrays are becoming more sensitive to SEE. At the same time, error correction is being used more aggressively in RHBD development. However, it is also true that control circuits are also becoming more sensitive. Control circuit errors will have to be mitigated at a higher system level.

V. Memory Trends

We reviewed memory technologies in general, for the purposes of identifying any trends that could be extracted for predicting future developments. We discuss a couple of these trends here.

A. STT-MRAM

Spin-Torque Transfer (STT) memory is a type of magnetic random access memory (MRAM) with limited radiation effects information available at this point. It is expected to perform quite well. We have identified significant performance capability – reaching cell-level performance capable of DDR3-like operation. Some manufacturers are pursuing densities that are sufficient to consider for this effort.

B. RRAM

Resistive RAM (RRAM) cells are inherently hard against single event effects. The control circuitry is the most problematic for SEE. In [11] the authors showed that SEFI could occur with sensitivity that is similar to what is seen in DRAMs. The authors also showed that in some cases power-cycling was required to recover operation. TID performance is not explicitly known, but because relatively large amounts of current are required to program bits, it is believed TID impact

on the cells will be minimized. Controlling the large currents on the die may result in poor TID performance in the peripheral circuitry (failures below 20-50 krad[Si] are expected for standard RRAM, though RHBD efforts can eliminate this limitation).

C. SRAM

There are currently no viable SRAMs with densities of interest to this work. The main problem with these devices for this study is that SRAMs require about 100 times as much power per bit as DRAM bits (~10 nW vs ~100 pW). For the non-synchronized devices, the another issue is decoding the address and returning data in the required timeframe. This memory type is tabled.

D. DRAM

DRAM devices have consistently increased SEFI sensitivity at advanced nodes, but individual cells have improved in SEE performance. DRAM devices can run from around 50 to well over 500 krad(Si) in terms of TID performance. The main trends moving forward are: controllers are prone to SEFI and getting worse, controllers are more and more complex, cells are inherently improving for both TID and SEE – but both must be verified in a given technology, devices with multiple voltage support are expected to have reduced TID performance. Some RHBD manufacturers are working with embedded DRAM (eDRAM) where the RHBD can be used to fabricate the controller, but findings have not been promising.

E. NAND FLASH

NAND Flash has significant endurance limitations and cannot meet the requirements of this program for volatile memory. For TID performance, the on-chip voltage generation has significant limitations and usually does not exceed 50 krad(Si) of tolerance. This memory type is tabled.

F. NOR FLASH

NOR Flash has similar endurance limitations to NAND Flash and cannot meet the requirements of this program. This memory type is tabled.

G. MRAM

Previous studies of MRAM have shown that the cells themselves are inherently rad hard, with no real evidence of SEEs in the cells. All data are limited by TID and SEE failures in the peripheral circuits and actual SEE and TID performance trends are hard to establish because no significant interest in MRAM radiation performance has been developed in the last 5 years. It is believed that appropriate control support should result in viable MRAMs for this program.

H. PCRAM

Phase change RAM cells are inherently rad hard. Similar to MRAM and FeRAM the radiation issue for PCRAM is the controller circuitry. There may also be problems cell endurance and integration densities. However this technology is not yet tabled in this effort.

I. FeRAM

Ferroelectric RAM is similar to MRAM in its inherent cell robustness to radiation. Similar to MRAM, the main issue with FeRAM is the ability to provide the required circuitry to support the cell architecture without the support circuitry introducing significant radiation sensitivity. FeRAM may be excluded from this study by other reasons, but is not tabled yet.

J. Other Memory Technologies

The following memory types were considered to be too preliminary, or too far away from the required application, at this stage to establish any radiation performance estimates.

A. 3D XPoint memory
B. Quantum dot memory
C. Nano-RAM (NRAM) – carbon nanotube memory
D. Molecular memory
E. Racetrack memory
F. Molecular nanowire memory
G. Write once, read many (WORM) memory
H. Flexible nonvolatile memory
I. Crossbar (1t1r) RRAM

VI. Packaging and Interconnects

The impact of radiation on devices comes from direct ionization in the case of lower energy particles. But for higher energy particles (generally above 100 MeV/nucleon), nuclear interactions can occur. In this case both the incident ion and the device atom are important. For this reason, modern packaging, which sometimes uses high atomic number materials such as tungsten, can cause high LET secondaries off of the packaging material to be a source for high LET ions in the device. An example of a high-z overlayer impacting the collected charge in proton secondary events, can be seen in **Error! Reference source not found.**. The use of high-Z materials can alter the secondary spectrum from proton and neutron interactions.

High-Z materials are used in connecting die across 2.5 and 3D-stacks in modern heterogeneous devices. The high-Z material can actually reach very high density in devices that could potentially have all the control circuitry on one die, but have interconnects to the other die that have the storage elements. This could be anywhere from 0.1% to nearly 100% of all storage cells having interconnects. And for 1 Gb parts, this could easily be as high as $1\times10_6$ high-Z interconnects.

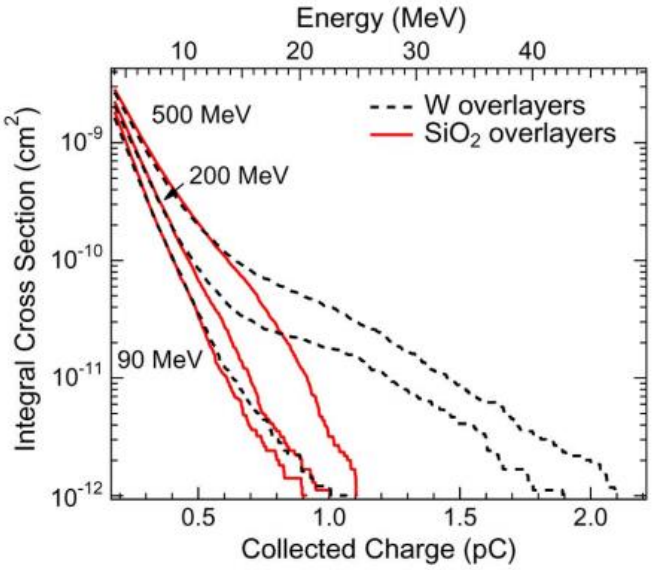

Figure 5: Effect of tungsten (W) overlayers in charge collected as a result of proton secondary recoil particles [6 Clemens 2010].

The primary area that this packaging issue is likely to impact is devices that are operating in proton environments. Generally, there are not a significant number of high energy protons except in trapped particle belts.

Although we have made a determination here that packaging materials may have a significant effect on the sensitivity of devices in higher energy environments, we do not have sufficient materials to establish guidelines or design rules.

VII. Conclusion

This paper details a study that formally reviewed RHBD and commercial technology through published materials. The study focused on determining what technologies may benefit from development in the next few years, to provide a memory device sufficient to support various programs. This paper is a presentation of this formal review effort of the existing materials.

The key findings are the following:

1. TID performance in commercial single-application devices with limited on-chip power development continues to improve (especially if chip-to-chip communication is performed at low operating voltage).
2. TID performance in embedded devices is unclear, with some heterogeneous devices performing considerably worse than the technology would otherwise indicate.
3. SEE in memory cells is generally not a major concern because devices can (and in many cases are) configured so that physically adjacent cells are not logically close – so if an ion changes two or more bits, they appear as multiple SBUs in unrelated error-correction regimes.
4. SRAM continues to be the worst performing memory cell architecture for SEE – especially with the recent improvements in DRAM cells.
5. Many devices are pushing system-level error correction requirements on users. This allows users to tailor error tolerance, but makes user designs more complex.
6. Devices tending towards increased complexity have controllers that contribute significantly to SEFI sensitivity. Thus, devices with more complex external interfaces, such as DRAM, or more complex internal operations, such as Flash, are at greater risk for SEFI.
7. Devices that have a need to push speed limits tend to have temporary data storage and/or control information stored in SRAM. (Recall that SRAMs are the worst performers for SEE). This includes NAND Flash which tries to speed up the transfer of data using SRAM buffers. This is important because SRAM cells are the worst performing, in terms of SEE, and require some sort of SEE mitigation.
8. RHBD, in the feature size required to achieve the desired density, has two significant problems that limit SEE performance – first, RHBD library elements are too small to easily separate redundant elements (of the library element), which is causing increased SEE sensitive (for example, in DICE cells) – and second, the actual storage elements are generally implemented in SRAM (though other macro cells exist, such as e-DRAM).
9. Significant proton sensitivity is expected in many devices, but it should be possible to harden controller chips to not have this problem.

VIII. Acknowledgment

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Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

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